Lab Exercise Two

**Step 1**

Write the SystemVerilog module for the Gray Code Converter that we developed in a previous class (10 pts).

Here are the simplified equations:

G = x

H = x’y + xy’

I = y’z + yz’

**Step 2**

Based on the following truth table create a self-checking testbench to test the SystemVerilog code created Step 1. The testbench must test all rows in the truth table (30 pts).

Hint: Use the 2x4 Decoder testbench covered in class on 10/12 as a guide.

